

What is claimed is:

1 1. A structure comprising a carrier foil; an electrically conductive layer on one
2 of the major surfaces of the carrier foil; a dielectric layer located on the electrically
3 conductive layer wherein the dielectric layer having circuitry features; and metal conductive
4 circuitry located within the circuitry features wherein the metal conductive circuitry is
5 substantially flush/coplanar with and surrounded by the dielectric layer.

1 2. The structure of claim 1 wherein the circuitry features in the dielectric layer
2 are formed completely thru it to the conductive layer.

1 3. The structure of claim 1 wherein the circuitry features in the dielectric layer
2 are formed short of the conductive layer.

1 4. The structure of claim 1 wherein the conductive circuitry comprised lines of
2 about 0.5 to about 1 mil wide and being about 0.5 to about 3 mils spaced apart.

1 5. The structure of claim 1 wherein the metal conductive circuitry comprise
2 copper.

1 6. The structure of claim 1 wherein the dielectric layer comprises an epoxy
2 resin or polyimide resin.

1 7. The structure of claim 1 wherein the carrier foil comprises copper.

1 8. The structure of claim 1 wherein the electrically conductive layer comprises
2 chromium.

1 9. The structure of claim 1 wherein the flush metal conductive circuitry is
2 covered with gold or nickel-gold.

1 10. The structure of claim 1 wherein the flush metal conductive circuitry is
2 selectively covered with gold or nickel-gold.

1 11. The structure of claim 10 wherein gold wire bond attach exist between gold
2 covered circuitry and other components or circuitry features attached to the structure.

1 12. The structure of claim 1 wherein a cavity exist thru the dielectric layer to the
2 electrically conductive layer wherein said cavity resides an electronic component.

1 13. The structure of claim 1 wherein the structure is attached to a stiffening
2 dielectric layer.

1 14. A structure comprising repetitive layers of a structure of claim 1 attached
2 together by a dielectric layer.

1 15. The structure of claim 14 comprising interconnects from any layer of a
2 conductive metal circuitry to any other layer of conductive metal circuitry.

1 16. The structure of claim 1 comprising flush metal conductive circuitry
2 interconnects from any via in the structure to any other via in the structure.

1 17. A structure comprising a dielectric base layer; a second dielectric layer
2 containing circuitry features located upon the base dielectric layer; and metal conductive
3 circuitry located within the circuitry features wherein the metal conductive circuitry is
4 substantially flush/coplanar with and surrounded by the second dielectric layer.

1 18. A structure comprising repetitive layers of the structure of claim 17 wherein
2 the conductive circuitry comprises lines of about 0.5 to about 1 mil wide and being about 0.5

1 27. The structure of claim 26 comprising interconnects from any layer of
2 conductive metal circuitry to any other layer of conductive metal circuitry.

1 28. The structure of claim 26 comprising flush metal conductive circuitry
2 interconnects from any via in the structure to any other via in the structure.

1 29. A structure comprising a dielectric base layer; a second dielectric layer
2 containing circuitry features located upon the base dielectric layer; and metal conductive
3 circuitry located within the circuitry features wherein the metal conductive circuitry is
4 substantially flush/coplanar with and surrounded by the second dielectric layer;
5 wherein the conductive circuitry comprises lines of about 0.5 to about 1 mil wide
6 and being about 0.5 to about 3 mils spaced apart and circuit features of sufficient size to
7 permit an electronic component to be located in said structure.

1 30. The structure of claim 29 wherein said electronic component is an integrated
2 circuit chip and wherein a cavity exists thru the dielectric layer to the metal conductive layer
3 and wherein said integrated circuit chip resides in said cavity.

1 31. The structure claim 30 wherein the flush metal conductive circuitry is
2 covered with gold or nickel-gold, and
3 wherein gold wire bond attach exists between gold covered circuitry and said
4 integrated circuit chip.

1 32. A method of fabricating a structure having embedded substantially flush/coplanar
2 circuitry features which comprises:
3 providing carrier foil having a top side and bottom side and an electrically
4 conductive blanket layer on said top side;
5 coating the electrically conductive layer with a dielectric material;

6 forming circuitry features in said dielectric material; and
7 plating conductive metal to fill said circuitry features.

1 33. The method of claim 32 which further comprises planarizing the side of the
2 structure containing said conductive metal to provide a planar surface having features of
3 conductive metal surrounded by dielectric material.

1 34. The method of claim 33, which further comprises the step of plating a
2 conductive finish metal layer onto said planar surface.

1 35. The method of claim 35 which further comprises blanket seeding the top
2 surface and circuit features in the dielectric material prior to plating the conductive metal.

1 36. The method of claim 35 wherein the conductive metal is blanket plated in
2 the seed layer followed by planarizing the conductive metal to provide a planar surface
3 having features of conductive metal surrounded by dielectric material.

1 37. The method of claim 32 wherein the circuitry features are formed through
2 the dielectric layer and up to the conductive layer exposes said layer.

1 38. The method of claim 32 wherein the circuitry features are formed in the
2 dielectric layer and short of the conductive layer.

1 39. The method of claim 33 wherein plating conductive metal is plated only in
2 the circuitry features.

1 40. The method of claim 8 which further comprises attaching the structure after
2 the planarizing to a substrate or dielectric.

1 41. The method of claim 39 which further comprises removing the carrier foil
2 while the conductive layer protects the conductive metal from being removed, and then
3 removing the conductive layer.

1 42. The method of claim 32 which comprises removing the carrier foil while the
2 conductive layer protects the conductive metal from being removed, and then removing the
3 conductive layer to form a smooth surface wiring on one side and a rough surface on
4 another side.

1 43. The method of claim 42, which further comprises the step of plating a
2 conductive finish layer such as gold, nickel gold or other precious metal onto said smooth
3 surface wiring.

1 44. The method of claim 42, which further comprises attaching the rough surface
2 to a dielectric material.

1 45. The method of claim 44 which further comprises attaching to a substrate.

1 46. The method of claim 36 which comprises joining at least two structures
2 having said embedded flush circuitry features together.

1 47. The method of claim 32 which further comprises blanket seeding the top
2 surface and circuit features in the dielectric material prior to plating the conductive metal;
3 planarizing the side of the structure containing said conductive metal to provide a
4 planar surface having features of conductive metal surrounded by dielectric material;
5 optionally joining at least two structures having said embedded flush circuitry
6 features together;

7 and removing the carrier foil while the conductive layer protects the conductive
8 metal from being removed, and then removing the conductive layer to form a smooth
9 surface wiring on one side and a rough surface on another side.

1 48. The method of claim 47 wherein the circuitry features are formed through
2 the dielectric layer and up to the conductive layer exposes said layer.

1 49. The method of claim 47 wherein the circuitry features are formed in the
2 dielectric layer and short of the conductive layer.

1 50. The method of claim 49 which further comprises attaching photoimageable
2 dielectric layer forming vias, blanket seeding and blanket plating a conductive metal;
3 selectively subtractive etching the blanket plating to form conductive
4 interconnections.

1 51. The method of claim 49 which further comprises attaching photoimageable
2 dielectric layer;
3 forming vias;
4 forming interconnection between vias;
5 blanket seeding and blanket plating a conductive metal; and
6 planarizing.

1 52. The method of claim 21 wherein the circuitry features are formed through
2 the dielectric layer and up to the conductive layer exposes aid layer;
3 and which further comprises plating a conductive material selectively onto the
4 underlying conductive layer;
5 planarizing the side of the structure containing metal to provide a planar
6 surface having features of conductive metal surrounded by dielectric material;
7 optionally joining at least two structures having said embedded flush
8 circuitry features together;
9 and removing the carrier foil while the conductive layer protects the
10 conductive metal from being removed, and then removing the conductive layer to form a
11 smooth surface wiring on one side and a rough surface on another side.

1 53. The method of claim 32 wherein the circuitry features are formed through
2 the dielectric layer and up to the conductive layer exposes said layer;

